# FSM based High Speed VLSI Architecture for DBUTVF Algorithm

# Abstract:

A Novel Finite state machine with data based VLSI architecture for fixed 3×3 kernal for Decision based unsymmetrical trimmed variants filter (DBUTVF) is proposed in this paper. The proposed architecture uses one hot encoding to assign the different states that were used in state diagram. A novel rank ordering algorithm that is better than its 1D counterpart is also a novel feature of this architecture. The architecture was targeted for the device XC3s5000-5fg900. The result of the architecture is evaluated in terms of area, speed and power for the targeted device.

**Tools used:**

**Xilinx13.2**